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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
12816-046US1

U.S. APPLICATION NO. (If Known, see 37 CFR 1.5)
10/089650

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/09412	26 September 2000	30 September 1999

TITLE OF INVENTION
PROTECTION CIRCUIT FOR AN ACCESS-ARBITRATED BUS SYSTEM NETWORK

APPLICANT(S) FOR DO/EO/US
Jens Barrenscheen, Mario Keil, Hermann Kern and Andreas Pechlaner

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. ☐ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☒ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern other documents or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:
    ☒ International Search Report
    ☐
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JC10 Rec'd PCT/PTO 01 APR 2002

APPLICATION NO (IF KNOWN)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
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7. ☒ The following fees are submitted:

	CALCULATIONS PTO USE ONLY	
Basic National Fee (37 CFR 1.492(a)(1)- (5)):		
Neither international preliminary examination fee (37 CFR 1.482) or international search fee (37 CFR 1.445(a)(2)) paid to USPTO nd International Search Report not prepared by the EPO or JPO..... **$1040**		
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ıternational preliminary examination fee paid to USPTO (37 CFR 1.482) ut all claims did not satisfy provisions of PCT Article 33(1)-(4)..... **$710**		
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Claims	Number Filed	Number Extra	Rate		
otal Claims	14 - 20 =		x **$18**	$0.00	
dependent Claims	2 - 3 =		x **$84**	$0.00	
ULTIPLE DEPENDENT CLAIMS(S) (if applicable)			+ **$280**	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$0.00	
] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are duced by 1/2.				$0.00	
SUBTOTAL =				$890.00	
ocessing fee of **$130** for furnishing the English Translation later than ☐ 20 ☐ 30 onths from the earliest claimed priority date (37 CFR 1.492(f))				$0.00	
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e for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be companied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$0.00	
TOTAL FEES ENCLOSED =				$890.00	
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☒ A check in the amount of $890.00 to cover the above fees is enclosed.
☐ Please charge my Deposit Account No. 06-1050 in the amount of $0.00 to cover the above fees. A duplicate copy of this sheet is enclosed.
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TE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.

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REGISTRATION NUMBER 42,729

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Attorney's Docket No.: 12816-046US1 / S1699 GC/sta

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Jens Barrenscheen et al. Art Unit : Unknown
Serial No. : N/A Examiner : Unknown
Filed : Herewith
Title : PROTECTION CIRCUIT FOR AN ACCESS-ARBITRATED BUS SYSTEM NETWORK

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the claims:

Cancel claims 1-11.

Add claims 12-25.

-- 12. A protective circuit comprising:

a logic isolation circuit to isolate a network section from a bus system network using logic when a fault state is recognized in the network section;

a first transceiver to connect to a first network section;

a second transceiver to connect to a second network section; and

wherein a first transceiver receiver in the first transceiver recognizes a fault state in the first network section, and a second transceiver receiver in the second transceiver recognizes a fault state in the second network section, and the logic isolation circuit includes logic signal inputs to connect to both receivers and logic signal outputs to connect to transceiver transmitters.

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Signature

Leroy Jenkins
Typed or Printed Name of Person Signing Certificate

13. The protective circuit of claim 12 wherein the logic isolation circuit comprises:

reception multiplexers having a first signal input connected to the first transceiver receiver and a second signal input receive a logically recessive transmission signal; and

transmission multiplexers having a signal output connected to one of the transceiver transmitters and a first signal input connected to a signal output of the reception multiplexers for the transceiver receiver, wherein a logically recessive transmission signal is applied to the second signal input of the transmission multiplexers.

14. The protective circuit of claim 12 wherein the logic isolation circuit blocks a dominant transmission signal from the network section.

15. The protective circuit of claim 12 wherein the logic isolation circuit blocks a dominant transmission signal to the network section.

16. The protective circuit of claim 12 further comprising a fault bus to connect the logic isolation circuit to control nodes in the bus system network, wherein the fault bus provides information data to the control nodes indicating that the network section recognized as faulty has been isolated from the bus system network.

17. The protective circuit of claim 13 wherein the first signal inputs of the transmission multiplexers is connected to the signal outputs of the reception multiplexers with DC decoupling.

18. A protective circuit for an access arbitrated bus system network, the protective circuit comprising:

a fault recognition device to recognize a fault state in a network section in the bus system network by monitoring voltage levels on bus lines in the bus system network; and

a switching device to isolate the network section from the bus system network by switching bus lines when a fault state has been recognized in the network section.

19. The protective circuit of claim 18 wherein the fault recognition device comprises:

a first fault state detection circuit to detect a fault state in a first network section;

a second fault state detection circuit to detect a fault state in a second network section; and

a fault recognition logic circuit connected to the first and the second fault state detection circuits which outputs a control signal to the switching device to isolate the first and the second network sections when the first or the second fault state detection circuits detect a fault state.

20. The protective circuit of claim 19 further comprising a fault bus to connect the logic isolation circuit to control nodes in the bus system network wherein the fault bus provides information data to the control nodes indicating that the network section recognized as faulty has been isolated from the bus system network.

21. The protective circuit of claim 18 wherein the access arbitrated bus system is a Controller Area Network (CAN) bus system.

22. The protective circuit of claim 18 wherein the access arbitrated bus system is a J 1850 bus system.

23. The protective circuit of claim 18 wherein the access arbitrated bus system is a Carrier Sense Multiple Access (CSMA) bus system.

24. The protective circuit of claim 18 wherein the fault recognition device recognizes as fault states, short circuits between the bus lines in a network section, short circuits between the bus lines in the network section and ground, and short circuits between the bus lines in the network section and supply voltage.

25. The protective circuit of claim 18 wherein the fault recognition device recognizes the termination of a fault state in a network section and actuates the isolation device to remove the isolation between the network sections and the overall bus system. --

Applicant :
Serial No. :
Filed :
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REMARKS

Applicant has cancelled claims 1-11 and added claims 12-25 to correct typographical errors and multiple dependencies.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be examined. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 4-1-02

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Version with markings to show changes made

In the claims:

Claims 1-11 have been cancelled.

Claims 12-25 have been added as follows:

-- 12. A protective circuit comprising:

a logic isolation circuit to isolate a network section from a bus system network using logic when a fault state is recognized in the network section;

a first transceiver to connect to a first network section;

a second transceiver to connect to a second network section; and

wherein a first transceiver receiver in the first transceiver recognizes a fault state in the first network section, and a second transceiver receiver in the second transceiver recognizes a fault state in the second network section, and the logic isolation circuit includes logic signal inputs to connect to both receivers and logic signal outputs to connect to transceiver transmitters.

13. The protective circuit of claim 12 wherein the logic isolation circuit comprises:

reception multiplexers having a first signal input connected to the first transceiver receiver and a second signal input receive a logically recessive transmission signal; and

transmission multiplexers having a signal output connected to one of the transceiver transmitters and a first signal input connected to a signal output of the reception multiplexers for the transceiver receiver, wherein a logically recessive transmission signal is applied to the second signal input of the transmission multiplexers.

14. The protective circuit of claim 12 wherein the logic isolation circuit blocks a dominant transmission signal from the network section.

15. The protective circuit of claim 12 wherein the logic isolation circuit blocks a dominant transmission signal to the network section.

16. The protective circuit of claim 12 further comprising a fault bus to connect the logic isolation circuit to control nodes in the bus system network, wherein the fault bus provides information data to the control nodes indicating that the network section recognized as faulty has been isolated from the bus system network.

17. The protective circuit of claim 13 wherein the first signal inputs of the transmission multiplexers is connected to the signal outputs of the reception multiplexers with DC decoupling.

18. A protective circuit for an access arbitrated bus system network, the protective circuit comprising:

a fault recognition device to recognize a fault state in a network section in the bus system network by monitoring voltage levels on bus lines in the bus system network; and

a switching device to isolate the network section from the bus system network by switching bus lines when a fault state has been recognized in the network section.

19. The protective circuit of claim 18 wherein the fault recognition device comprises:

a first fault state detection circuit to detect a fault state in a first network section;

a second fault state detection circuit to detect a fault state in a second network section; and

a fault recognition logic circuit connected to the first and the second fault state detection circuits which outputs a control signal to the switching device to isolate the first and the second network sections when the first or the second fault state detection circuits detect a fault state.

20. The protective circuit of claim 19 further comprising a fault bus to connect the logic isolation circuit to control nodes in the bus system network wherein the fault bus provides information data to the control nodes indicating that the network section recognized as faulty has been isolated from the bus system network.

21. The protective circuit of claim 18 wherein the access arbitrated bus system is a Controller Area Network (CAN) bus system.

22. The protective circuit of claim 18 wherein the access arbitrated bus system is a J 1850 bus system.

23. The protective circuit of claim 18 wherein the access arbitrated bus system is a Carrier Sense Multiple Access (CSMA) bus system.

24. The protective circuit of claim 18 wherein the fault recognition device recognizes as fault states, short circuits between the bus lines in a network section, short circuits between the bus lines in the network section and ground, and short circuits between the bus lines in the network section and supply voltage.

25. The protective circuit of claim 18 wherein the fault recognition device recognizes the termination of a fault state in a network section and actuates the isolation device to remove the isolation between the network sections and the overall bus system. --

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Description

Protective circuit for an access arbitrated bus system network

The invention relates to a protective circuit for an access arbitrated bus system network for isolating a faulty network section from the overall network.

A bus comprises a plurality of parallel lines for data transmission which connect various functional units in a multiplex mode. On a bus, a plurality of functional units can receive data simultaneously, but only one functional unit can serve as a sender of information data at any particular time. An access arbitrated bus system is a bus system in which a plurality of users have transmission authority for transmission to the bus, the current transmission authorization being defined by the bus access. Examples of access arbitrated bus systems are CAN bus systems (CAN: Controller Area Network), J 1850 bus systems or bus systems operating on the basis of the CSMA method. The CSMA method (CSMA: Carrier Sense Multiple Access) is an access method for access with equal authorization to a plurality of stations or control nodes connected to the bus.

The CAN bus system is a bus system network, covering an area, for connecting locally disposed control nodes which is increasingly being used in vehicles, in particular. The individual control nodes are connected to one another via the CAN bus system and can interchange data frames via the bus lines. In this context, the data frames have a functional identification which identifies the vehicle function addressed, such as oil, brake, light or the like. One option for fault monitoring is to ascertain a particular CAN control node which is provided for

controlling a particular vehicle control function and monitors the bus lines to determine whether an associated data frame is available for this function. If the CAN control node does not receive the required information within a particular time period, an emergency mode is activated.

Figure 1 shows a CAN bus system based on the prior art. As per the example shown in figure 1, the CAN bus system comprises three CAN control nodes CAN1, CAN2, CAN3 which are connected by means of connecting lines a1, b1, a2, b2, a3, b3 to a first CAN bus line having a low level CANL and to a second CAN bus line having a high level CANH. The voltage level difference between the high level bus line CANH and the low level bus line CANL reproduces the transmitted information. As soon as the level difference exceeds a particular voltage threshold value, this is interpreted as a logic high bit, and as soon as the voltage level difference falls below a threshold value, this is interpreted as a logic low bit.

Various fault states can arise in the CAN bus system, namely a short circuit between the two CAN bus lines, a short circuit between one of the two bus lines CANL or CANH and ground, and a short circuit between one of the two bus lines CANL, CANH and a supply voltage V_{BB}. If the CAN bus system based on the prior art, as shown in figure 1, is installed in a motor vehicle, the various fault states can be caused by an accident. If, by way of example, the control node CAN1 is a control node for a distance radar situated in the vehicle's bumper, an accident involving a collision may result in a short circuit between the two connecting lines a1, b1. This fault state is recognized by all the control nodes in the bus system, which prevents further data interchange via the bus.

It is therefore the object of the present invention to provide a protective circuit for an access arbitrated bus system network which prevents failure of the overall bus system network in the event of a short circuit occurring on a bus line.

The invention achieves this object by means of a protective circuit having the features specified in patent claim 1.

The invention provides a protective circuit for an access arbitrated bus system network having:
a fault recognition device for recognizing a fault state in a network section in the overall bus system network and having
an isolation device for isolating the network section from the overall bus system network when a fault state is recognized in the network section.

Preferred developments of the inventive protective circuit are specified in the subordinate subclaims.

In one preferred development of the inventive protective circuit, the fault recognition device monitors voltage levels on the bus lines in the bus system network in order to recognize a fault state.

This affords the particular advantage that the network section recognized as being faulty is isolated with a very short reaction time, since physical voltage levels are monitored directly and no long-lasting transmission protocol queries are made.

The isolation device is preferably a logic isolation circuit which uses logic to isolate the network section recognized as being faulty from the rest of the bus system network.

The logic isolation circuit isolates the network section recognized as being faulty from the bus system preferably by blocking the dominant transmission signal from or to the network section.

In one preferred development of the inventive protective circuit, the logic isolation circuit is connected to the rest of the control nodes in the bus system network via a fault bus, the fault bus providing the control nodes with information data indicating that the network section recognized as being faulty is isolated from the overall bus system network.

In another preferred development of the inventive protective circuit, the fault recognition device has a first fault state detection circuit for detecting a fault state in a first network section, a second fault state detection circuit for detecting a physical fault state in a second network section and a fault recognition logic circuit which is connected to the two fault state detection circuits and outputs a control signal to the isolation device for the purposes of isolating the two network sections when a fault state is detected by one of the two fault state detection circuits.

The isolation device is preferably a switching device for switching the bus lines in the bus system network.

In another preferred development of the inventive protective circuit, the fault recognition logic circuit is connected to control nodes in the bus system network via a fault bus, the fault bus providing the control nodes with information data indicating that the network section recognized as being faulty is isolated from the overall bus system network.

In another preferred development of the inventive protective circuit, the protective circuit has a first transceiver for connection to a first network section, a second transceiver for second connection to a second network section, and a logic isolation circuit, where the transceiver receiver in the first transceiver is provided for recognizing a fault state in the first network section, and the transceiver receiver in the second transceiver is provided for recognizing a fault state in the second network section, and where the logic isolation circuit has logic inputs connected to the transceiver receivers and logic outputs connected to the transceiver transmitters.

In one preferred embodiment of the inventive protective circuit, the logic isolation circuit has two reception multiplexers, whose first input is respectively connected to a transceiver receiver and whose second input respectively has a logically recessive transmission signal applied to it, and two transmission multiplexers, whose output is respectively connected to a transceiver transmitter, whose first input is respectively connected to the output of the reception multiplexer in the transceiver receiver in the other transceiver and whose second input respectively has a logically recessive transmission signal applied to it.

Preferably, the first input of a transmission multiplexer is connected to the output of a reception multiplexer with DC decoupling.

In one preferred embodiment, the first input of the transmission multiplexer and the output of the reception multiplexer are respectively DC-decoupled by an interposed optocoupler.

The inventive protective circuit is preferably provided for a CAN bus system, a J 1850 bus system or a CSMA bus system.

In one preferred development of the inventive protective circuit, the fault recognition device recognizes as fault states short circuits between the lines in a network section, short circuits between the lines in the network section and ground, and short circuits between the lines in a network section and a supply voltage.

In one preferred development of the inventive protective circuit, the fault recognition device recognizes the termination of a fault state in a network section and actuates the isolation device to remove the isolation between the network sections and the overall bus system.

Preferred embodiments of the inventive protective circuit are described below with reference to the appended drawings in order to explain features which are fundamental to the invention.

In the drawings:

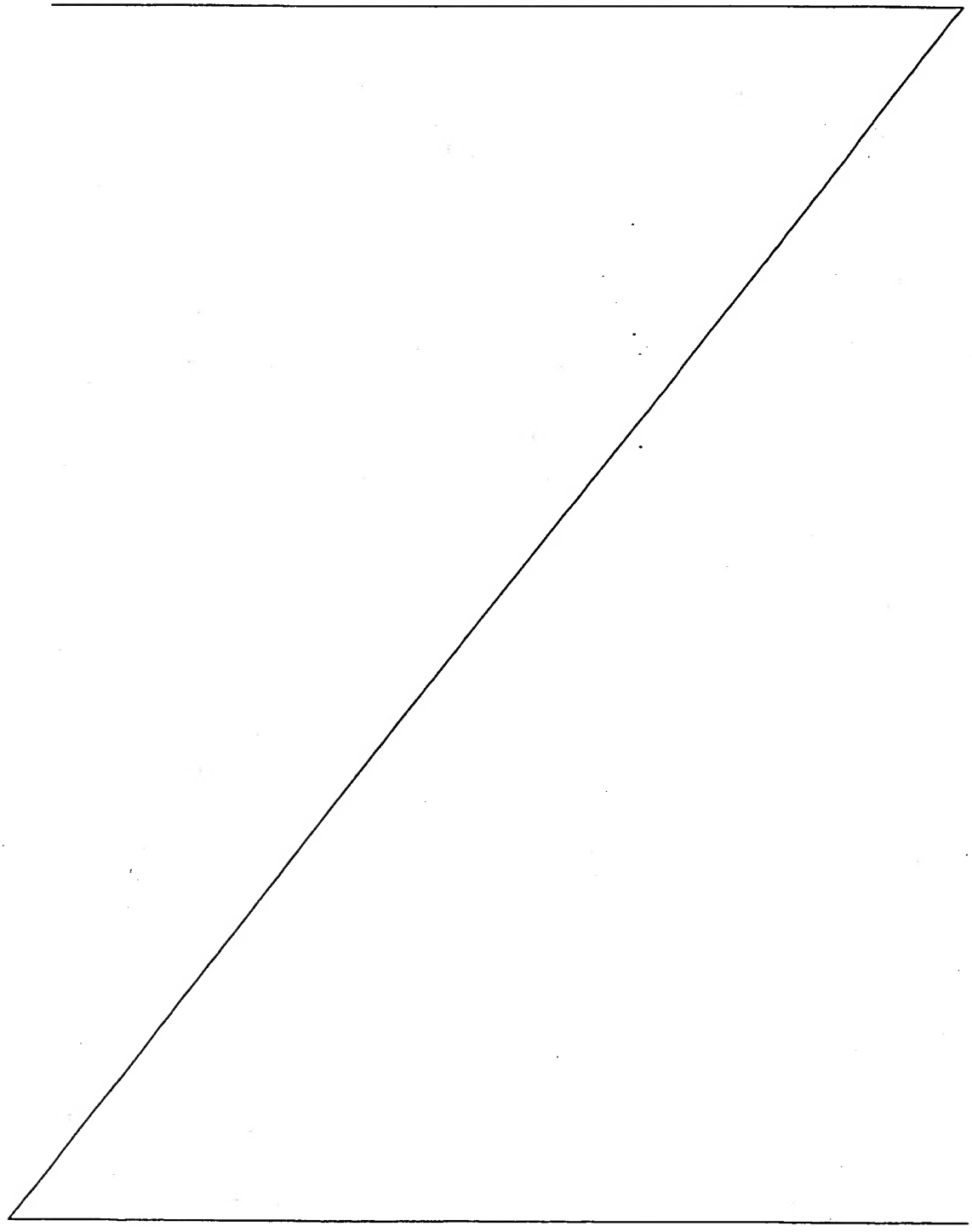
figure 1 shows a CAN network based on the prior art;

figure 2 shows a CAN bus system network with a first embodiment of the inventive protective circuit;

figure 3 shows a CAN bus system network with a second embodiment of the inventive protective circuit;

figure 4 shows the isolation device for isolating the network sections in the second embodiment of the inventive protective circuit, shown in figure 3.

Figure 2 shows a CAN bus system network with a first



11. The CAN bus lines 1b, 2b are connected to CAN bus line connections 13b, 14b for the inventive protective circuit 12.

In the inventive protective circuit 12 based on the first embodiment, the fault recognition device has a first fault state detection circuit 15 for detecting a fault state in the first network section and a second fault state detection circuit 16 for detecting a fault state in the second network section. The outputs of the two fault state detection circuits 15, 16 are connected to a fault recognition logic circuit 19 via lines 17, 18. When a fault state is detected in one of the two network sections by one of the two fault state detection circuits 15, 16, the fault recognition logic circuit 19 outputs a control signal via a control switching line 20 to a switching device 21 for the purpose of switching internal bus lines 1c, 2c within the protective circuit 12, the internal bus lines 1c, 2c respectively connecting the bus line connections 14a, 14b and 13a, 13b to one another. The switching device 21 has a plurality of switches 22, 23 connected in parallel, with a respective switch being provided for each bus line 1c, 2c. The switches 22, 23 are preferably semiconductor switches which block in both signal directions in the off state. The semiconductor switches preferably comprise two reverse-connected series MOSFET transistors whose forward resistance is less than 10 Ω.

The fault state detection circuits 15, 16 detect short circuits between the lines in a network section, for example between the connecting lines 6, 7 for the control node 3 in the first network section, as a first fault state.

In the example shown in figure 2, the first network section can be a network section which is arranged in

the external region of a vehicle body. In this case, an accident may result in a short circuit between the connecting lines 6, 7 for the control node 3. This short circuit is detected by the fault state detection circuit 15 using resistors (not shown). In addition, the two fault state detection circuits 15, 16 recognize as a second fault state a short circuit between the bus lines in the two network sections and ground or earth, and a short circuit between the bus lines in the two network sections and a supply voltage V_{BB}.

The two fault state detection circuits 15, 16 detect a fault state which has arisen in one of the two network sections by directly monitoring physical voltage levels, and not using bus data protocol queries. This means that a fault state which has arisen can be detected very quickly, and the two network sections are isolated from one another by the inventive protective circuit 12 within a very short reaction time of below 10 µs.

The fault recognition logic circuit 19 receives fault recognition signals from the two fault state detection circuits 15, 16 via the control lines 17, 18 and performs a logic OR operation. As soon as a fault state arises in one of the two network sections, the two switches 22, 23 in the switching device 21 are turned off by the fault recognition logic circuit via the switching control line 20, and the two network sections are isolated from one another.

When the two switches 22, 23 have been turned off and the two network sections have been isolated, the fault recognition device in the inventive protective circuit 12 can recognize in which of the two network sections the fault state has occurred. If the fault state detection circuit 15 continues to output a fault state detection signal to the fault recognition logic circuit

19 via the line 17 after the two switches 22, 23 have turned off, while at the same time the fault state detection circuit 16 outputs no fault recognition signal to the fault recognition logic circuit 19 via the fault recognition line 18, then the fault recognition logic circuit 19 recognizes that the fault state has arisen in the first network section. If, conversely, the fault state detection circuit 15 reports no fault state after the switches 22, 23 have turned off, while at the same time the fault state detection circuit 16 continues to report a fault state, the fault recognition logic circuit 19 recognizes that the fault has arisen in the second network section.

The fault recognition logic circuit 19 is preferably connected to the microprocessors 3b, 4b, 5b in the CAN control nodes 3, 4, 5 via an additional fault bus line 24. The fault bus line 24 provides the control nodes 3, 4, 5 in the two network sections with information data indicating that a network section recognized as being faulty is isolated from the overall bus system network. With a multiplicity of network sections, the control nodes are additionally informed about which network section has had the fault state arise in it on a local basis.

Figure 3 shows a second embodiment of the inventive protective circuit 12. In the case of the second embodiment of the inventive protective circuit, shown in figure 3, the two network sections are not isolated physically by splitting the bus line, but rather are isolated using logic. The protective circuit 12 based on the second embodiment has a first transceiver 25 for connection to the bus lines 1a, 2a in the first network section via the bus line connections 13a, 14a, and also a second transceiver 26 for connection to the bus lines 1b, 2b in the second network section via the bus line connections 13b, 14b. The transceivers 25, 26 each have

transceiver transmitter parts 25-S, 26-S and transceiver receiver parts 25-E, 26-E. The two transceiver transmitter parts 25-S, 26-S are connected to a logic isolation circuit 29 via lines 30, 31. The transceiver receiver parts 25-E and 26-E in the two transceivers 25, 26 are connected to the logic isolation circuit 29 via lines 27, 28.

Figure 4 shows the circuit design of a preferred embodiment of the logic isolation circuit 29 in the case of the second embodiment of the inventive protective circuit 12, as shown in figure 3.

The logic isolation circuit 29 preferably contains four multiplexers, namely two reception multiplexers 32, 33 and two transmission multiplexers 34, 35. Each of the multiplexers 32, 33, 34, 35 has two respective signal inputs, a signal output and a control line connection. The first signal input 36 of the reception multiplexer 32 is connected to the transceiver receiver part 25-E via the line 27, with a recessive transmission signal from the access arbitrated bus system network which is to be protected being applied to the second signal input 37.

A CAN network has two transmission signal states, namely a logic high level recessive transmission signal state and a logic low level dominant transmission signal state. In the quiescent state, the logic high level recessive transmission signal state is present on the bus line, while active data transmission uses both the low level dominant transmission signal state and the high level transmission signal state. In a CAN bus system, the second signal input 37 of the reception multiplexer 32 thus has a logically recessive high level transmission signal applied to it which is indicated by a logic H in figure 4.

The first signal input 38 of the second reception multiplexer 33 is connected to the transceiver receiver part 26-E via the line 28. The second signal input 39 of the second reception multiplexer 33 likewise has a logically recessive data transmission signal applied to it.

The signal output 40 of the first reception multiplexer 33 is connected via a line 41 to the first signal input 42 of the transmission multiplexer 35, whose second signal input 43 receives a logically recessive transmission signal. The signal output 44 of the transmission multiplexer 35 is connected to the transceiver receiver part 26-S via the line 31.

The signal output 45 of the reception multiplexer 33 is connected via a line 46 to the first signal input 47 of the transmission multiplexer 34, whose second signal input 48 receives a logically recessive transmission signal. The signal output 49 of the transmission multiplexer 34 is connected to the transceiver transmitter part 25-S via the line 30.

The reception multiplexer 32 is switched via a control line 50 which is connected to the output line 30 of the transmission multiplexer 34. The transmission multiplexer 34, for its part, is controlled via a control line 51 which receives the signal produced at the output connection 40 of the reception multiplexer 32 as control signal.

The reception multiplexer 33 is controlled via a control line 52 which is connected to the output connection 44 of the transmission multiplexer 35. The transmission multiplexer 35 receives its control signal via a control line 53 which is connected to the output connection 45 of the reception multiplexer 33.

The reception multiplexer 32 receives a received signal RxD1 from the receiver 25 via the signal line 27. The reception multiplexer 33 receives a received signal RxD2 from the transceiver 26 via the line 28. Conversely, the transmission multiplexer 34 outputs a transmitted signal TxD1 to the transceiver 25 via the line 30, and the transmission multiplexer 35 outputs a transmitted signal TxD2 to the transceiver 26 via the signal line 31.

The table below shows the transmitted and received signals in the logic isolation circuit 29 for the various operating situations B in the bus system.

Operating situation B	RxD1	RxD2	TxD1	TxD2
B1 Quiescent state	1	1	1	1
B2 Transmitter in network section A	0	0	①	0
B3 Transmitter in network section B	0	0	0	①
B4 Transmitter in both network sections	0	0	①	①
B5 Fault in network section A	1/0	x	①	①
B6 Fault in network section B	x	1/0	①	①

Table 1

In this context, ① signifies a high level recessive signal which is output in order to prevent a deadlock state. A ⓪ arises as a consequence of the transmission of a dominant bus state.

In operating situation B1, the entire bus system is in the quiescent state. In operating situation B2, a control node in a first network section A is transmitting, so that the reception multiplexer 32 receives via the line 27 a dominant low level transmitted signal 0 which is forwarded via the line 31 as transmitted signal TxD2.

If, conversely, the second network section B is transmitting, the logic isolation circuit 29 receives a logically dominant 0 signal via the circuit 28 and forwards it on the line 30 to the first network section A via the transceiver 25. From the operating situations B4, B5, B6, the two network sections A, B are isolated by logic such that no dominant logic low level data transmission signals are connected by the isolation circuit 29, but instead a blocking signal is inevitably produced. In this case, the signal outputs 44, 49 of the two transmission multiplexers 35, 34 are set to the recessive high level data transmission signal.

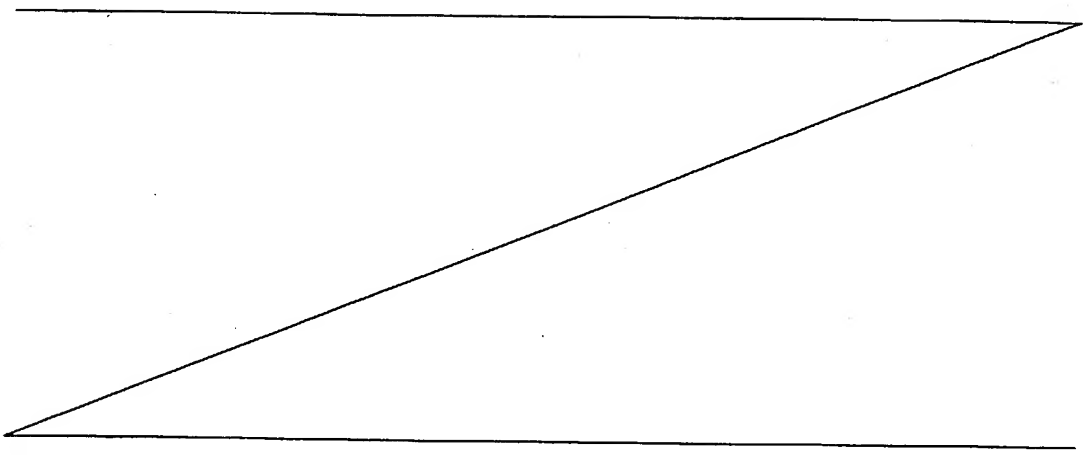
The table below shows the transmitted and received signals in a control node 3 in the first network section A and a control node 4 in a second network section B for the various operating situations B.

The control node 3 transmits a transmitted signal S_1 and receives a received signal E_1. The control node 4 transmits a transmitted signal S_2 and receives a received signal E_2.

Operating situation B	S_1	S_2	E_1	E_2
B1 Quiescent state	1	1	1	1
B2 Transmitter in network section A	0	1	0	0
B3 Transmitter in network section B	1	0	0	0
B4 Transmitter in both network sections	0	0	0	0
B5 Fault in network section A	x	0/1	x	S_2
B6 Fault in network section B	0/1	x	S_1	x

Table 2

In one preferred development of the logic isolation circuit 29 shown in figure 4, the signal input 42 of the transmission multiplexer 35 is connected to the signal output 40 of the reception multiplexer 32 with DC decoupling. In addition, the first signal input 47



The logic isolation circuit 29 is connected to the control nodes 3, 4, 5 via a fault bus line 24 in order to transmit information data.

As can be seen from figure 2 and figure 3, both embodiments of the inventive protective circuit are of symmetrical design, which means that the inventive protective circuit 12 can be used in bus lines 1, 2, with the bus line connection 14a being able to be interchanged with the bus line connection 14b, and the bus line connection 13a being able to be interchanged with the bus line connection 13b. Preferably, the bus line connections 13a, 14a and the bus line connections 13b, 14b can also be interchanged when the protective circuit 12 is inserted into the bus system network. This affords the particular advantage of simple assembly.

The inventive protective circuit 12 is distinguished by very low circuit complexity, which facilitates its design using standard chips. The inventive protective circuit can be used universally in all access arbitrated bus system networks, such as a CAN bus system, a J 1850 bus system or a CSMA bus system. It can be interposed at any points within the bus system network. The direct monitoring of the physical level state on the bus lines means that the inventive

protective circuit 12 is distinguished by a very short reaction time of less than 10 µs. Another advantage of the inventive protective circuit is that the faulty network section can be located, with this also being communicated to bus system control nodes via a fault bus 24. When the fault state has been terminated, the inventive protective circuit 12 automatically removes the isolation of the network sections again.

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List of reference symbols:

1a, 1b, 1c	Bus line
2a, 2b, 2c	Bus line
3	Control node
4	Control node
5	Control node
3a	Transceiver
4a	Transceiver
5a	Transceiver
3b	Microcomputer
4b	Microcomputer
5b	Microcomputer
3c	Transmission conductor
4c	Transmission conductor
5c	Transmission conductor
3d	Reception line
4d	Reception line
5d	Reception line
6	Connecting lines
7	Connecting lines
8	Connecting lines
9	Connecting lines
10	Connecting lines
11	Connecting lines
12	Protective circuit
13a	Bus line connections
13b	Bus line connections
14a	Bus line connections
14b	Bus line connections
15	Fault state detection circuit
16	Fault state detection circuit
17	Fault state detection line
18	Fault state detection line
19	Fault recognition logic circuit
20	Switching control line
21	Switching device
22	Switch

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23	Switch
24	Fault bus
25	Transceiver
26	Transceiver
27	Line
28	Line
29	Logic isolation circuit
30	Conductor
31	Conductor
32	Reception multiplexer
33	Reception multiplexer
34	Transmission multiplexer
35	Transmission multiplexer
36	Signal input
37	Signal input
38	Signal input
39	Signal input
40	Signal output
41	Line
42	Signal input
43	Signal input
44	Signal output
45	Signal output
46	Line
47	Signal input
48	Signal input
49	Signal output
50	Multiplexer control line
51	Multiplexer control line
52	Multiplexer control line
53	Multiplexer control line

Patent Claims

1. A protective circuit for an access arbitrated bus system network having:
a logic isolation circuit (29) for isolating a network section from the overall bus system network using logic when a fault state is recognized in the network section,
a first transceiver (25) for connection to a first network section and
a second transceiver (26) for connection to a second network section,
wherein
the transceiver receiver (25-E) in the first transceiver (25) is provided for recognizing a fault state in the first network section, and the transceiver receiver (26-E) in the second transceiver (26) is provided for recognizing a fault state in the second network section, and the logic isolation circuit (29) has logic signal inputs for connection to the transceiver receivers (25-E, 26-E) and also logic signal outputs for connection to the transceiver transmitters (25-S, 26-S).

2. The protective circuit as claimed in claim 1,
wherein
the logic isolation circuit (29) has two reception multiplexers (32, 33), whose first signal input (36, 38) is respectively connected to a transceiver receiver (25-E, 26-E) and whose second signal input (37, 39) respectively receives a logically recessive transmission signal, and
two transmission multiplexers (34, 35), whose signal output (49, 44) is respectively connected to a transceiver transmitter (25-S, 26-S) and whose first signal input (47, 42) is respectively connected to a signal output (40, 45) of the reception multiplexer

(32, 33) for the transceiver receiver (25-E, 26-E) in the other transceiver, with a respective logically recessive transmission signal being applied to the second signal input of the two transmission multiplexers (34, 35).

3. The protective circuit as claimed in claim 1 or 2, wherein
the logic isolation circuit (29) isolates the network section recognized as being faulty from the bus system by blocking a dominant transmission signal from or to the network section.

4. The protective circuit as claimed in claim 1, 2 or 3,
wherein
the logic isolation circuit (29) is connected to control nodes (3, 4, 5) in the bus system network via a fault bus (24), the fault bus (24) providing the control nodes (3, 4, 5) with information data indicating that the network section recognized as being faulty is isolated from the overall bus system network.

5. The protective circuit as claimed in one of the preceding claims,
wherein
the first signal input (47, 42) of the transmission multiplexers (34, 35) is respectively connected to the signal outputs of the reception multiplexers (32, 33) with DC decoupling.

6. A protective circuit for an access arbitrated bus system network having:
a fault recognition device (15, 16, 19) for recognizing a fault state in a network section in the overall bus system network by monitoring the voltage levels on the

bus lines (1a, 1b, 2a, 2b) in the bus system network and

a switching device (21) for isolating the network section from the overall bus system network by switching bus lines (1c, 2c) when a fault state is recognized in the network section.

7. The protective circuit as claimed in claim 6, wherein

the fault recognition device (15, 16, 19) has a first fault state detection circuit (15) for detecting a fault state in a first network section,

a second fault state detection circuit (16) for detecting a fault state in a second network section and

a fault recognition logic circuit (19) which is connected to the two fault state detection circuits (15, 16) and outputs a control signal to the isolation device for the purposes of isolating the two network sections when a fault state is detected by one of the two fault state detection circuits (15, 16).

8. The protective circuit as claimed in claim 7, wherein

the fault recognition logic circuit (19) is connected to control nodes in the bus system network via a fault bus (24), the fault bus (24) providing the control nodes (3, 4, 5) with information data indicating that the network section recognized as being faulty is isolated from the overall bus system network.

9. The protective circuit as claimed in one of the preceding claims,

wherein

the access arbitrated bus system is a CAN bus system, a J 1850 bus system or a CSMA bus system.

10. The protective circuit as claimed in one of the preceding claims,
wherein
the fault recognition device recognizes as fault states short circuits between the bus lines in a network section, short circuits between the bus lines in the network section and ground, and short circuits between the bus lines in the network section and a supply voltage.

11. The protective circuit as claimed in one of the preceding claims
wherein
the fault recognition device recognizes the termination of a fault state in a network section and actuates the isolation device to remove the isolation between the network sections and the overall bus system.

S0321

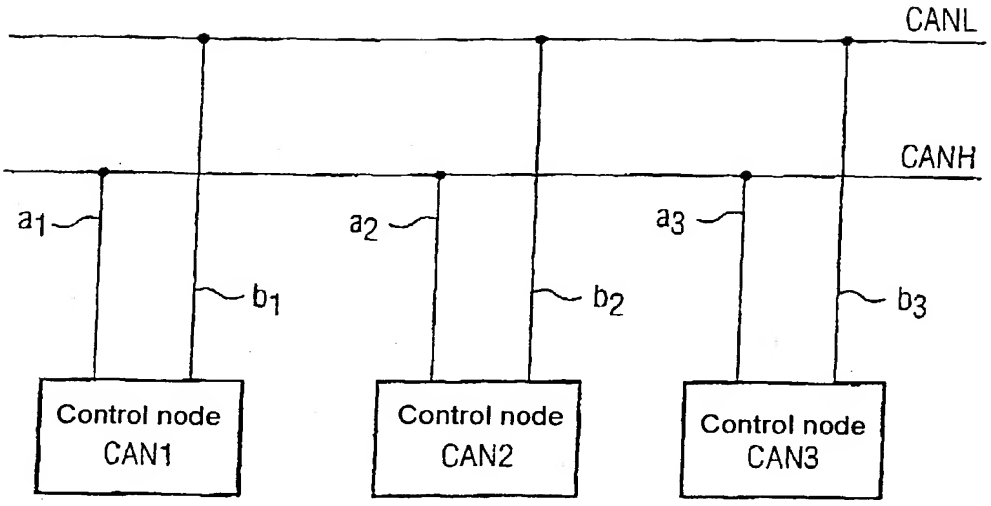
Abstract

Protective circuit for an access arbitrated bus system network

A protective circuit (12) for an access arbitrated bus system network having a fault recognition device for recognizing a fault state in a network section in the overall bus system network and an isolation device for isolating the network section from the overall bus system network when a fault state is recognized in the network section.

Figure 2

FIG 1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CANH
a1
a2
a3
b1
b2
b3
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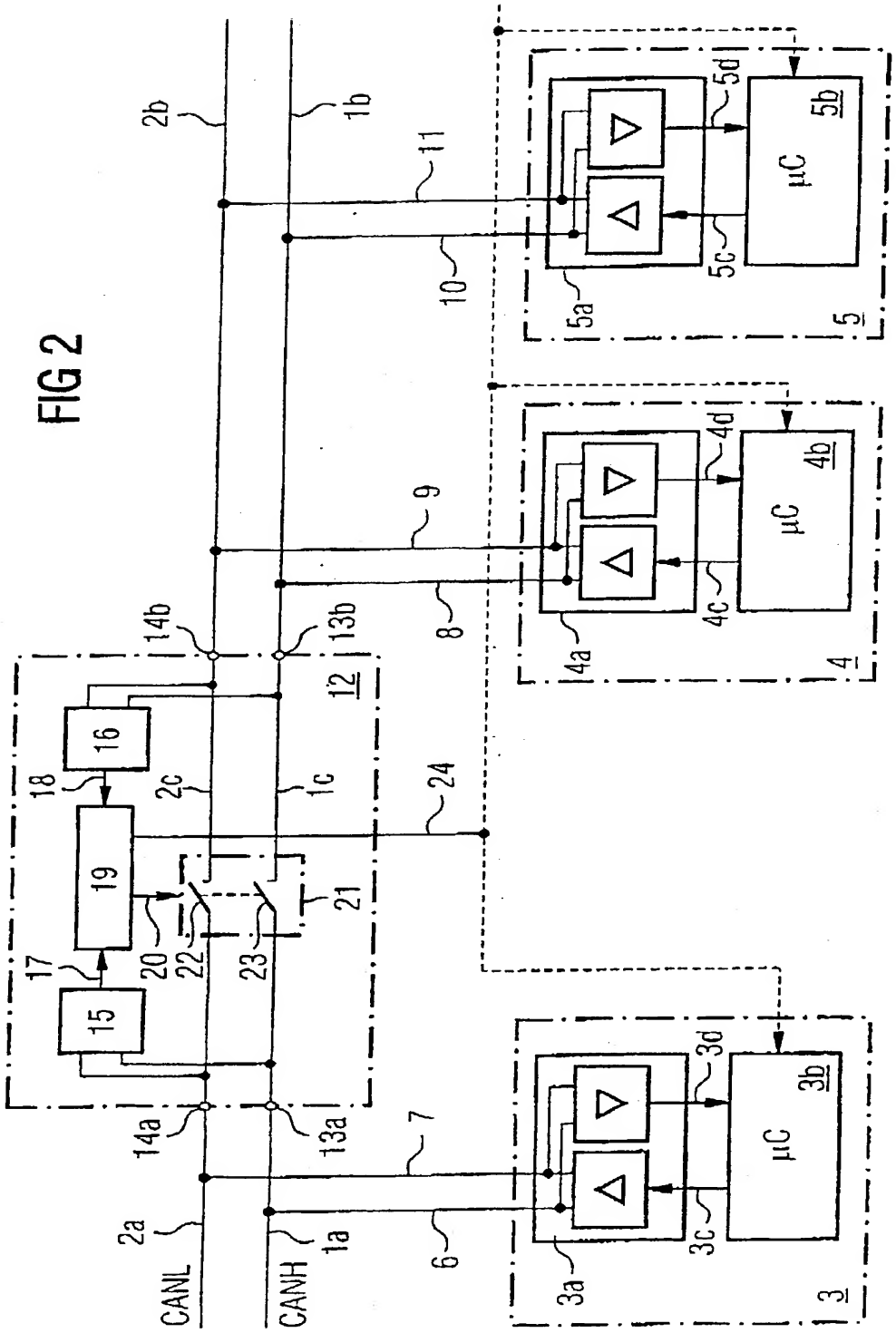
Control node CAN2
Control node CAN3

FIG 2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10
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5b
µC
5c
5a
5
9
8
4d
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µC
4c
4a
4
14b
13b
12
16
18
2c
1c
24
19
21
17
20
22
23
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13a
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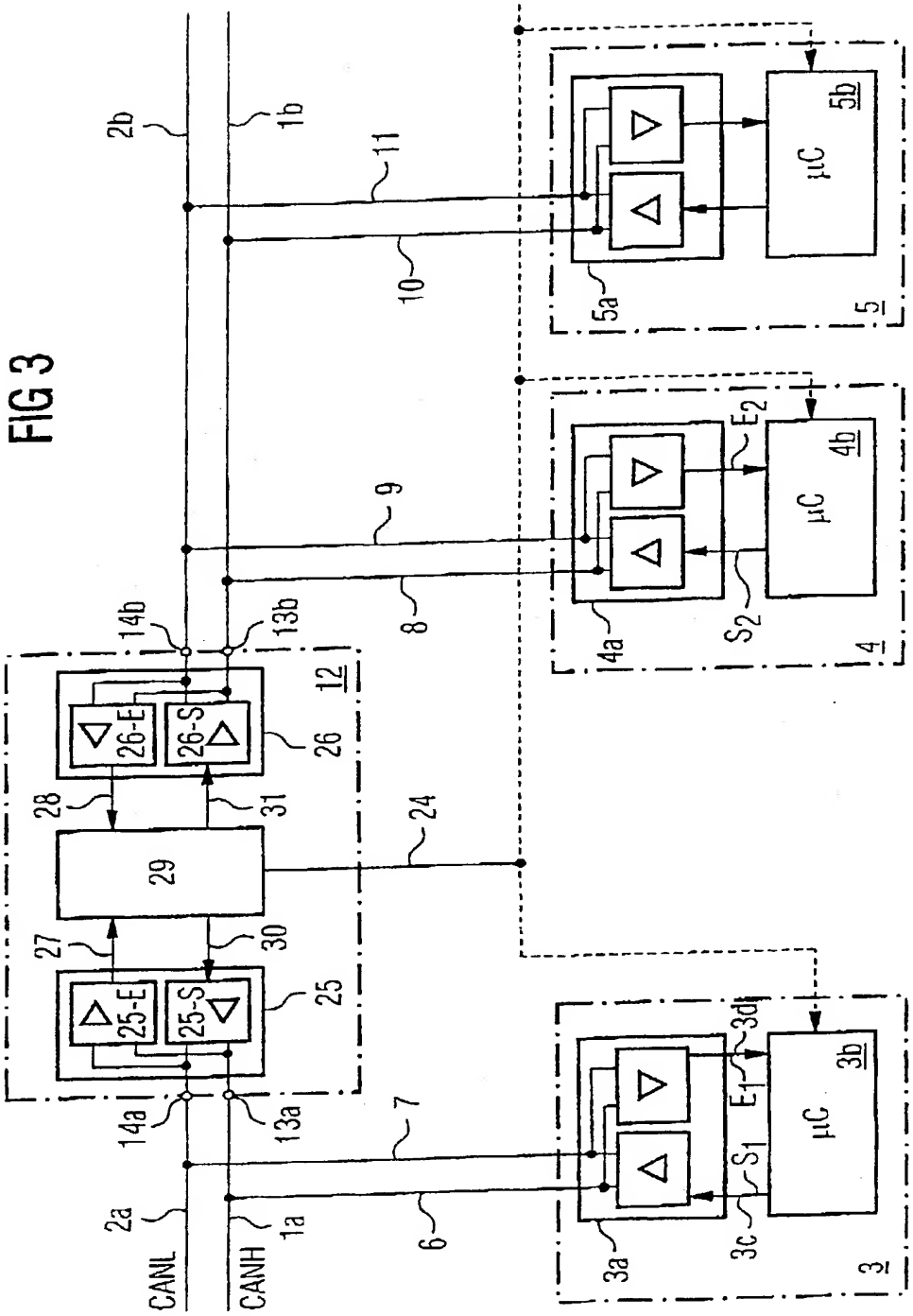
µC
3c
3a
3
2a
1a
6
CANL
CANH

FIG 3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µC
5b
4
4a
S2
E2
4b
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8
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26-E
26-S
26
28
31
24
29
27
30
25
25-E
25-S
14a
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7
6
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CANH
3
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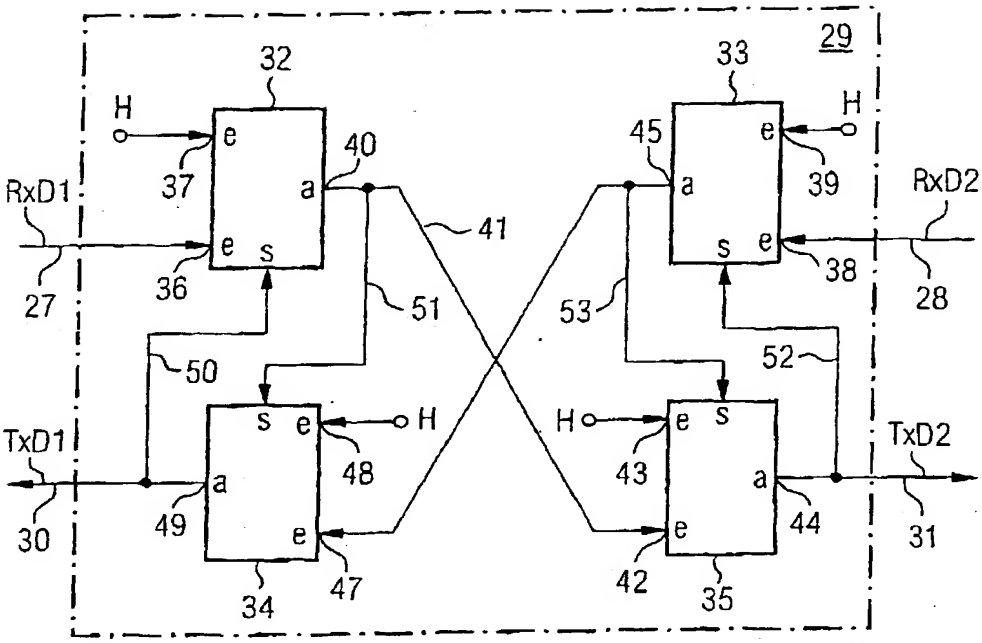
3c
S1
E1
3d
3b

FIG 4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RxD2
41
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36
38
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28
51
53
50
52
TxD1
TxD2
48
43
49
44
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42
34
35

Attorney's Docket No.: 12816-046US1
Client's Ref. No.: S1699 GC/sta

COMBINED DECLARATION AND POWER OF ATTORNEY

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Germany	19946993.8	September 30, 1999	[] Yes [X] No

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Faustino A. Lichauco, Reg. No. 41,942
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Citizenship: Germany
Post Office Address: Bgm. Drexler-Bogen 4, 82291 Mammendorf, Germany

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Inventor's Signature: A. Pechlaner Date: 16. APR. 2002
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Inventor's Signature: Hermann Kern Date: 4.17.2002
Residence Address: Bgm. Drexler-Bogen 4, 82291 Mammendorf, Germany
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